4.4 A Blocker Filtering Technique for Wireless Receivers

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In most wireless receivers a very stringent blocking requirement must be met. For instance, in the GSM standard, a desired signal 3dB above the sensitivity could be accompanied by a 0dBm blocker as close as 80MHz to the edge of the PCS band. Since the desired signal is weak, the LNA gain must be kept high, and thus the blocker must be filtered prior to reaching to the amplifier output. On the other hand, due to the modest Q of on-chip inductors, it is not practical to integrate such a sharp filter. For these reasons, all the existing receivers inevitably use an external surface acoustic wave (SAW) filter at the LNA input. This has several disadvantages. First, it increases the cost, especially in multi-mode multi-band applications. Secondly, the insertion loss of the SAW filter, typically as high as 3dB, degrades the receiver sensitivity. Third, it creates less flexibility to share the LNA in multi-band applications, and particularly in *software-defined radios*. In this paper, an on-chip filtering technique based on a feed-forward cancellation is presented which eliminates the need for a SAW filter in the receiver input.

The idea of blocker cancellation through feed-forward injection is not practical, as it requires a sharp notch filter to distinguish the desired signal from the blocker. The notch filter requirements are as stringent as the input SAW filter, and thus, it cannot be implemented on-chip. On the other hand, the filtering could be performed much more efficiently at *IF* through *downconversion*. This new concept is shown in Fig. 4.4.1, where the desired signal accompanied by the blocker is downconverted to a zero or low IF by the same LO signal used in the main receive path. The desired signal is now at or near DC, and is easily removed by a high-pass filter (HPF), while the blocker located at least a few tens of MHz away passes through. The same LO upconverts the blocker back to RF and subtracts it at the LNA output. As a result of this, an arbitrarily sharp frequency response is created, whose bandwidth and slope are simply controlled through adjusting the HPF characteristics. The HPF corner needs to be high enough to filter the desired signal, but sufficiently low to pass the blocker. Since the desired signal is around DC, whereas the blocker is at least several tens of MHz away, this is easily met.

The resulting RF filter pass-band always moves with the desired signal, that is, it is centered at the LO frequency. Thus, despite its narrow bandwidth, it does not affect the desired band. This could be thought of as a *receiver translational loop*, where the frequency response of the IF filter is translated to RF through downconversion. Similar to the transmitter, the resulting sharp frequency response at RF eliminates the need for a SAW filter at front-end.

To prove this concept, the LNA architecture shown in Fig. 4.4.2 is fabricated and measured. Since a quadrature LO signal is available in the receiver, the filtering path exploits single sideband I/Q mixers. A power detector at the LNA output activates the filtering only when a strong blocker is present. Thus, the extra power consumption as a result of the filtering circuits is practically negligible.

To achieve the desired attenuation in practice, the phase and gain of the filtering path must be well matched to that of the main signal. Due to the quadrature mixing in the filtering path, the switching gain of the cascade of downconversion and upconversion mixers is equal to *unity* as $Sin^2\theta+Cos^2\theta$ is equal to one. Thus, only the transconductance stage of the first mixer needs to be matched to that of the LNA. The phase mismatch arises from the delay introduced in the HPF, as well as the one created due the mixer limited bandwidth. To avoid this, the HPF corner must be well below the blocker frequency, and the mixers must be designed for sufficiently wide bandwidth.

Another practical concern arises from the noise figure degradation resulting from the injection circuitry. However, this is not an issue for several reasons. First, the filtering devices are turned off in the normal receive mode, and are only active when the blocker is present. Fortuitously, the receiver noise figure can be typically relaxed by 3dB in the presence of a blocker. For instance, in GSM, assuming a signal-to-noise ratio of 9dB is required at the baseband, the receiver blocking noise figure is relaxed to 13dB. Secondly, the noise created at the output of the first mixer experiences the same filtering just like the signal does. Thus, it is only the upconversion mixer that contributes noise to the LNA output and is minimized by proper design.

The LNA circuit is shown in Fig. 4.4.3. Despite its higher noise figure, a common-gate design is chosen for two reasons. First, although the filtering attenuates the blocker at the output, the LNA input must be able to tolerate a large signal. Since the common-gate LNA has no gain at the input, it is a desirable choice compared to an inductively degenerated common-source amplifier. Second, the common-gate design has a wide input bandwidth, and allows the inputs of different bands to be shared, eliminating the need for a switch in multi-band applications. A cascode structure is used for better isolation between the input and output ports. Moreover, it provides a low impedance node, suitable to inject the second mixer output current for blocker subtraction. The LNA measured noise figure is 3.9dB. Even though this is higher than what is typically achieved [1], it is still advantageous once the 3dB loss of the SAW filter and the switch is included. The LNA is tuned to 1.96GHz and has a measured passband gain of 23.4dB. Its input return loss remains less than –10dB over a wide frequency range of almost 1GHz.

Illustrated in Fig. 4.4.4, the downconversion mixer is a fully differential active circuit. It uses grounded-source devices at the input for better linearity, with a 12dB capacitive attenuation to reduce the blocker. The size of the input devices is optimized for the best linearity, and is chosen such that the overall transconductance of the mixer matches to that of the LNA input devices. The output employs a cascode current source, providing a *current* to the second mixer, which is a *current-mode passive* circuit [2] with a blocking capacitor at its input. The passive design ensures that the noise contribution of the second mixer is minimal.

The measured and simulated frequency response of the amplifier with and without filtering is shown in Fig. 4.4.5. The measurement results agree well with simulations and a stopband attenuation of more than 21dB is achieved. With the filtering enabled, the LNA gain is 20.9dB in the passband and achieves a noise figure of 6.8dB, 2.9dB higher than the LNA noise figure with no filtering. The LNA gain versus the blocker power is shown in Fig. 4.4.6. The gain stays relatively flat up to a blocker level of as high as 0dBm.

The test chip is fabricated in a 65nm CMOS technology and it occupies an active area of $0.28mm^2$. The die micrograph is shown in Fig. 4.4.7. The LNA is biased at 8mA and each of the active mixers drain 10.5mA.

References:

[1] O.E. Erdogan, R. Gupta, D.G. Yee, et al., "A Single-Chip Quad-Band GSM/GPRS Transceiver in 0.18μm Standard CMOS," *ISSCC Dig. Tech. Papers*, pp. 318-319, Feb., 2005

[2] M. Valla, G. Montagna, R. Castello, et al., "A 72-mW CMOS 802.11a Direct Conversion Front-End With 3.5-dB NF and 200-kHz 1/f Noise Corner," *IEEE J. Solid-State Circuits*, vol. 40, pp. 970-977, 2005.

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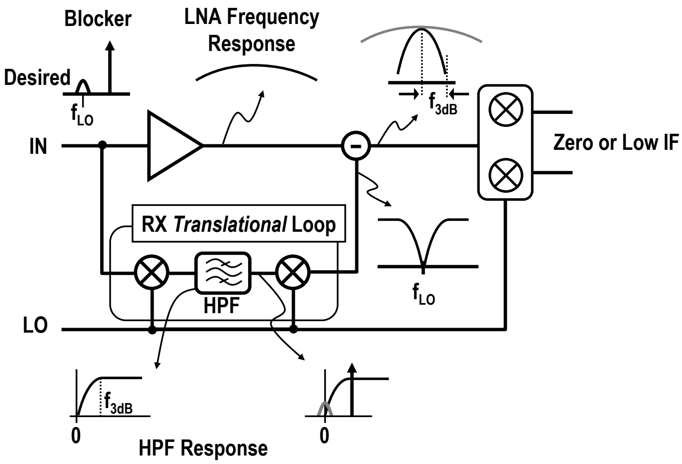

Figure 4.4.1: Concept of receiver translational loop.

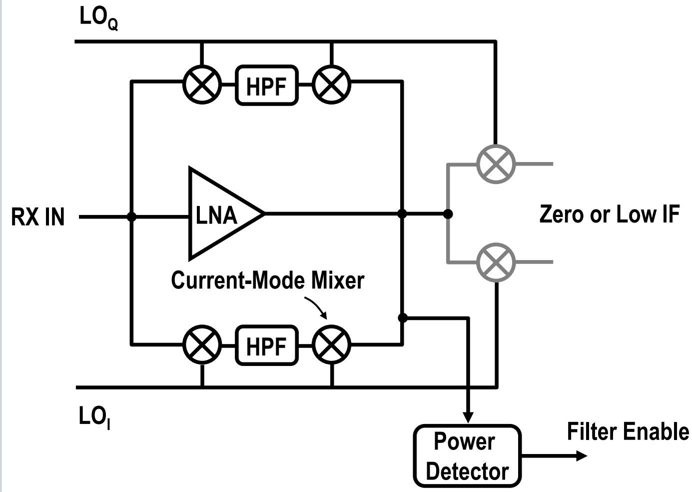

Figure 4.4.2: Architecture of the LNA with blocker filtering.

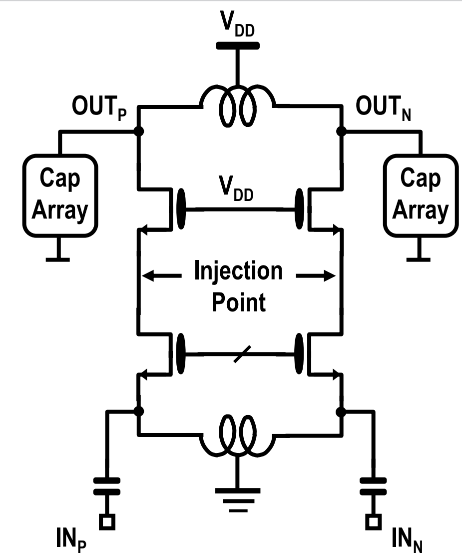

Figure 4.4.3: The LNA circuit.

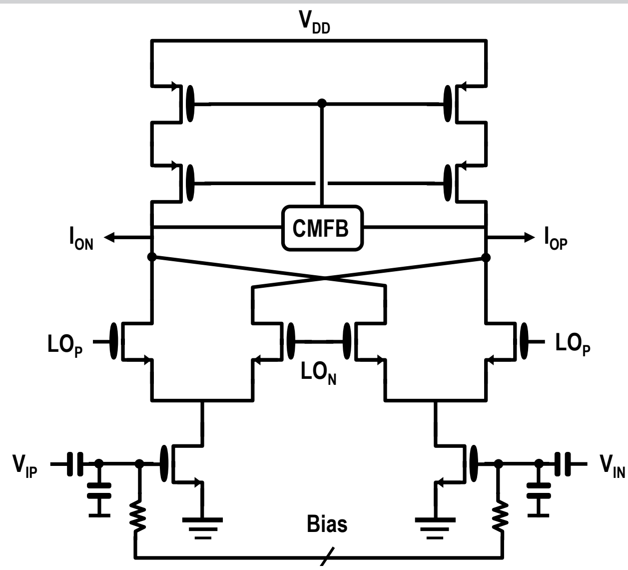

Figure 4.4.4: Circuit diagram of the first mixer.

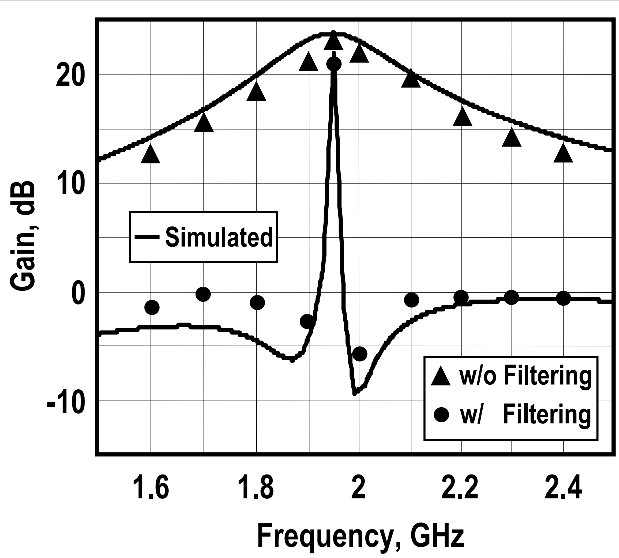

Figure 4.4.5: LNA measured and simulated frequency response.

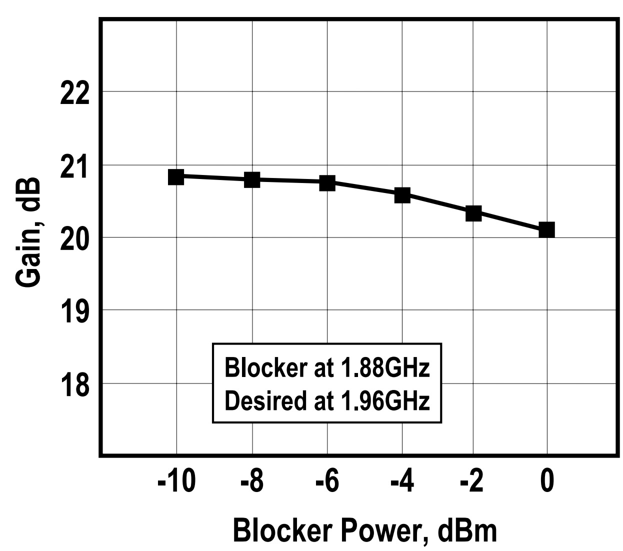

Figure 4.4.6: Measured LNA gain versus blocker power.

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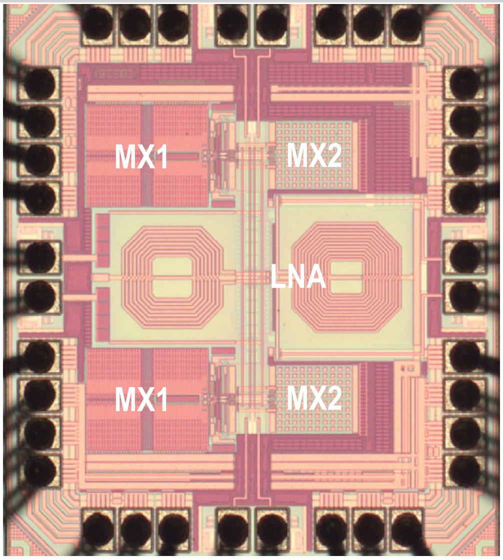

Figure 4.4.7: Die micrograph.